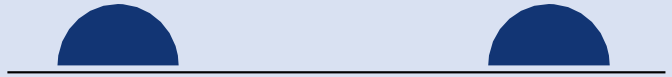
Kioxia NAND Flash Reliability Note

UD info
www.udinfo.com.tw

pSLC

NAND Types		Structure	Reliability (P/E Cycles)	Cost
2D	SLC		60000	$ $ $ $ $
	pSLC		30000	$ $ $ $
	MLC		3000	$ $
3D	TLC		3000	$
	pSLC		30000 +	$ $ $

- pSLC is the perfect solution for **heavy write application** with great performance.
- **Best Reliability to Cost (RTC) ratio**

3D TLC Solutions

NAND Types		Structure	Reliability (P/E Cycles)	Cost
2D	MLC		3000	$ $
3D	TLC		3000	$
	pSLC		30000 +	$ $ $

- 3D TLC Flash is **the current mainstream for industrial grade storage** in stead of MLC.
- UD info has implement Kioxia 3DTLC Flash with Phison's controller into **major product lines** with **aggressive price.**
- Operating Temp supports to **-40 to +85 c**

24nm SLC NAND Flash Reliability Note

- **Write/ Erase Endurance**
  - Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

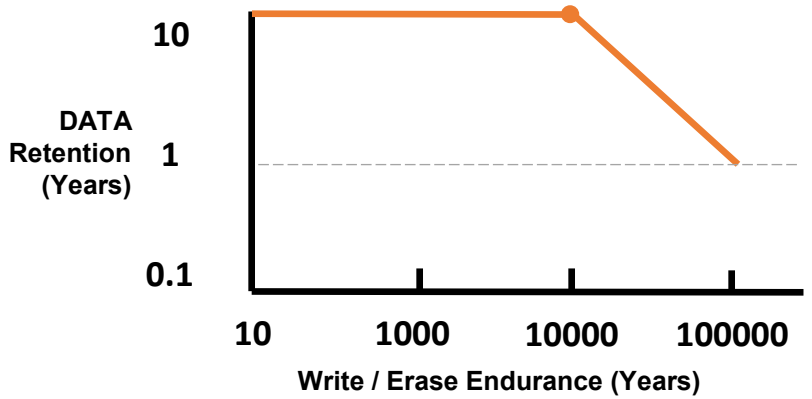
SLC	Write/ Erase Cycles (Cycles)	Cumulative Block Failure Rate
	100,000	Less than 0.04

- **Data Retention**
  - The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erase and reprogramming, the block may become usable again.

- **Here are the combined characteristics of Write/Erase Endurance and Data Retention.**

Write Erase Cycles (Cycles)	Estimated Data Retention (Year)
Initial (less than 100)	10
30,000	3
100,000	1

Condition of Data Retention Estimate:
- Vcc = 3.3V, Ta= 40 c, ECC= 40bit/1KB
- All Pages in blocks are tested with Random data
- DUT = Kioxia 24nm SLC



15nm MLC NAND Flash Reliability Note

- **Write/ Erase Endurance**
  - Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

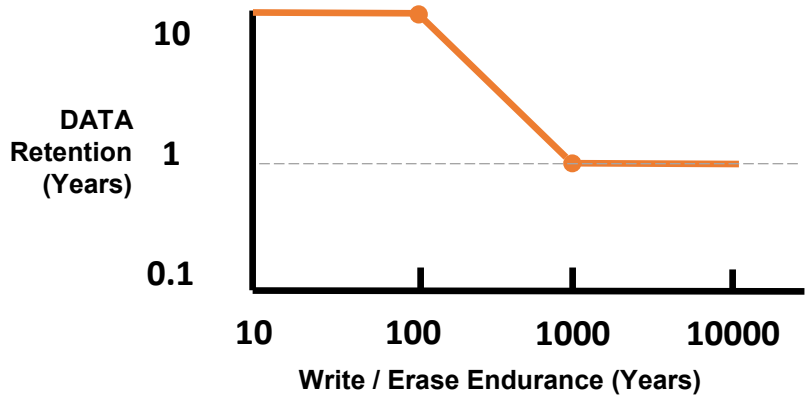
MLC	Write/ Erase Cycles (Cycles)	Cumulative Block Failure Rate
	3,000	Less than 0.04

- **Data Retention**
  - The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erase and reprogramming, the block may become usable again.

- **Here are the combined characteristics of Write/Erase Endurance and Data Retention.**

Write Erase Cycles (Cycles)	Estimated Data Retention (Year)
Initial (less than 100)	10
3,000	1

Condition of Data Retention Estimate:
- Vcc = 3.3V, Ta= 40 c, ECC= 40bit/1KB
- All Pages in blocks are tested with Random data
- DUT = Kioxia 15nm MLC



15nm Pseudo SLC (pSLC) Reliability Note

- **Write/ Erase Endurance**
  - Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

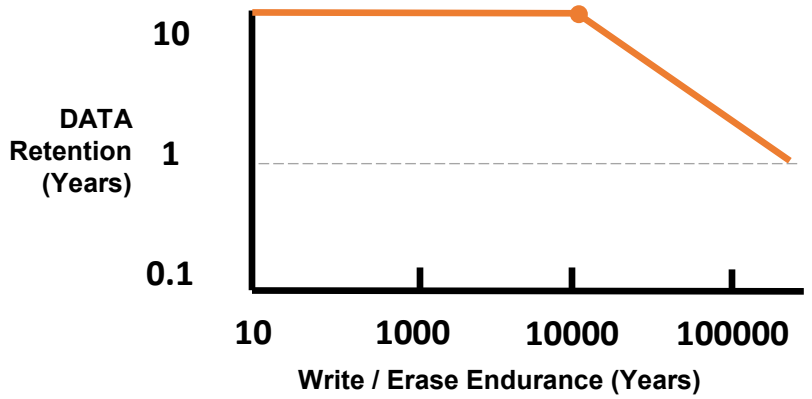
pSLC	Write/ Erase Cycles (Cycles)	Cumulative Block Failure Rate
	30,000	Less than 0.04

- **Data Retention**
  - The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erase and reprogramming, the block may become usable again.

- **Here are the combined characteristics of Write/Erase Endurance and Data Retention.**

Write Erase Cycles (Cycles)	Estimated Data Retention (Year)
Initial (less than 100)	10
30,000	1

Condition of Data Retention Estimate:
- Vcc = 3.3V, Ta= 40 c, ECC= 40bit/1KB
- All Pages in blocks are tested with Random data
- DUT = Kioxia 15nm pSLC



Bics3 3D TLC NAND Flash Reliability Note

- **Write/ Erase Endurance**
  - Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

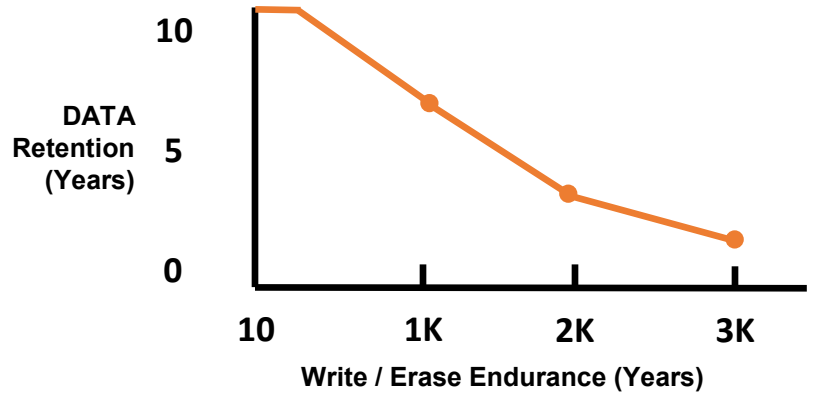
Bic3 3DTLC	Write/ Erase Cycles (Cycles)
	3,000

- **Data Retention**
  - The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erase and reprogramming, the block may become usable again.

- **Here are the combined characteristics of Write/Erase Endurance and Data Retention.**

Write Erase Cycles (Cycles)	Estimated Data Retention (Year)
Initial (less than 100)	10
3,000	1

Condition of Data Retention Estimate:
- DUT = S11 + Kioxia 3D TLC (BiCS3)
- Tc=40 c, LDPC
- All Pages in blocks are tested with Random data



Bics3 3D pSLC NAND Flash Reliability Note

- **Write/ Erase Endurance**
  - Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

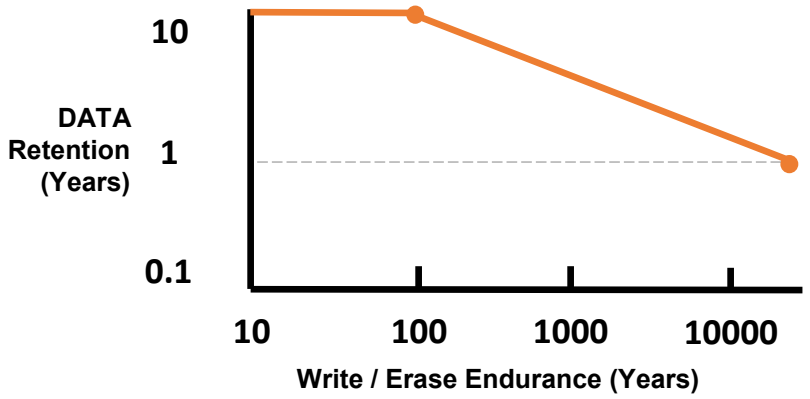
Bic3 3D pSLC	Write/ Erase Cycles (Cycles)
	30,000

- **Data Retention**
  - The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erase and reprogramming, the block may become usable again.

- **Here are the combined characteristics of Write/Erase Endurance and Data Retention.**

Write Erase Cycles (Cycles)	Estimated Data Retention (Year)
Initial (less than 100)	10
30,000	1

Condition of Data Retention Estimate:
- DUT = S11 + Kioxia BiCS3 pSLC
- VCC=3.3V, Tc=40 c, LDPC
- ECC(Hard-Bit)=200bits/4KB
- ECC(Soft-Bit)=380bits/4KB
- All Pages in blocks are tested with Random data



THANK YOU